

REMARKS

Claims 1-10 and 14-21 are pending.

Claims 1, 2 and 5 are amended. The amendments are being made for clarity and not patentability purposes, and no new matter is being added.

In section 8 of the Office Action, informalities have been identified in relation to Claims 1, 2 and 5. Appropriate corrections have been made in relation to these claims.

In section 9 of the Office Action, Claims 1-7, 9, 14, 15, 17 and 20 are rejected under 35 USC § 102(b) as being anticipated by US patent No. 5,996,057 (hereinafter referred to as "the Scales, III et al. patent"). Applicants are traversing this rejection.

The application contains three independent claims, namely Claims 1, 2 and 5. Below, Applicants explain that the Scales, III et al. patent does not disclose all of the elements of Claims 1, 2 and 5.

The Scales, III et al. patent relates to a data processing system (col. 2, line 59). According to col. 2, lines 60-66 of Scales, III et al. the data processing system allows the specification of 3 input operands comprising 2 input vectors and a control vector. The input operands are loaded into vector registers and a Permute-With- Replication (PWR) operation is performed on the 2 input vectors in a manner specified by the control vector. The result of the PWR operation is stored as an output operand in an output register.

The precise configuration of the data processing system disclosed in Scales, III et al. patent is described further at col. 5, lines 31-48. In particular, col. 5, lines 33-34, the system comprises a vector register file 200 having 32 vector registers. The vector register file 200 is coupled to a combine network 210 (col. 5, lines 35-36). The vector register file 200 provide 3 vectors (A, B and C) from 3 pre-selected or programmed registers of the vector register file 200 (col. 5, lines 36-38). The PWR operation is performed by the combine network 210, and the vector register file 200 includes a control register containing the control vector (col. 5, lines 46-47).

The above system is configured in a manner consistent with the description of FIG. 1 of the present application, which addresses known art.

Claim 1 recites, *inter alia*, the following features:

- a permutation logic block coupled to receive and permute vectors from at least one vector register according to control parameters;

- a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and
- control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

The Scales, III et al. patent does not teach “control means coupled between the plurality of control registers and the permutation logic block” as recited in Claim 1. The control registers of the Scales, III et al. patent are part of the vector register file 200.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 1.

Claims 3, 4, and 8-10 depend from Claim 1. By virtue of this dependence, Claims 3, 4 and 8-10 are also novel over the Scales, III et al. patent.

Amended Claim 2 provides for a single-instruction multiple-data microprocessor vector permutation system comprising control means coupled between the plurality of control registers and the permutation logic block. As explained above in support of Claim 1, the Scales, III et al. patent does not disclose control means coupled between the plurality of control registers and the permutation logic block. Accordingly, the Scales, III et al. patent does not anticipate Claim 2.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 2.

Claims 14-18 depend from Claim 2. By virtue of this dependence, Claims 14-18 are also novel over the Scales, III et al. patent.

Amended Claim 5 provides for a method for permutation in a single-instruction multiple-data microprocessor where control means are provided between the plurality of control registers and the permutation logic block. As explained above in support of Claim 1, the Scales, III et al. patent does not disclose control means coupled between the plurality of control registers and the permutation logic block. Accordingly, the Scales, III et al. patent does not anticipate Claim 5.

In view of the reasoning provided above, Applicants submit that the Scales, III et al. patent does not anticipate Claim 5.

Claims 6, 7, and 19-21 depend from Claim 5. By virtue of this dependence, Claims 6, 7, and 19-21 are also novel over the Scales, III et al. patent.

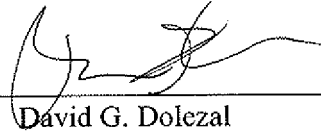
The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

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